CLAIMS

1. A semiconductor memory device comprising

a memory cell array containing plural memory cells which are arranged in the form of a matrix between plural bit line pairs divided into plural blocks each comprising a prescribed number of bit line pairs and plural word lines,

plural bit line selector circuits which are provided in correspondence to the aforementioned respective plural blocks so as to select 1 bit line pair from the aforementioned prescribed number of bit line pairs and electrically connect said selectable bit line pair to an output line pair,

plural bit line charge circuits which charge each of the aforementioned plural output line pairs to a prescribed signal level,

plural amplifier circuits which amplify the difference in the signal levels generated on the aforementioned respective plural output line pairs according to data stored in the selected memory cell,

a block selector circuit which selects one of the aforementioned plural output line pairs provided in correspondence to the aforementioned plural blocks according to a block selection signal and electrically connects said selected output line pair to a selectable output line pair, and

a data latch circuit which latches output data when the signal level of the aforementioned selective output line pair is not a complementary signal level and outputs first data or second data corresponding to the complementary signal level, either a first or a second complementary signal level, indicated by the signal level of the aforementioned selectable output line pair.

2. The semiconductor memory device of Claim 1, in which

the aforementioned block selector circuit has plural gate circuits connected between the aforementioned plural output line pairs and the aforementioned selectable output line pair, and

the aforementioned plural gate circuits have first and second switch circuits connected between one side of the aforementioned output line pair and the other side and between one side of the aforementioned selectable output line pair and the other side, in order to control the aforementioned first and second switch circuits to conduct or not conduct in accordance with a control signal.

3. The semiconductor memory device of Claim 2, in which the aforementioned first and the second switch circuits are transfer gates.

4. The semiconductor memory device of Claim 1, in which

the aforementioned block selector circuit has plural gate circuits connected between the aforementioned plural output line pairs and the aforementioned selectable output line pair,

the aforementioned plural gate circuits have first and second inverter circuits connected between one side of the aforementioned output line pair and the other side and between one side

of the aforementioned selective output line pair and the other side, respectively, in order to control the aforementioned first and the second inverter circuits to output either an output signal corresponding to an input signal or a high-impedance signal in response to a control signal.

5. The semiconductor memory device of Claim 4, in which the aforementioned first and the second inverter circuits are clocked inverter circuits.

6. The semiconductor memory device of Claim 1 in which the aforementioned plural bit line selector circuits have first and second data write circuits connected to one side and the other side of the aforementioned prescribed number of bit line pairs, and the aforementioned first and the second data write circuits supply complementary signals to one side and the other side of the aforementioned bit line pair in response to a write signal.

7. The semiconductor memory device of Claim 6, in which the aforementioned first and the second data write circuits are configured with first and second transistors connected respectively between one side of the aforementioned bit line pair and a power supply terminal.